Amendments to the Claims:

Please amend the claims as follows:

1-17. (Canceled)

18. (Currently Amended) A memory module, comprising:

~~a plurality of memory devices; and~~

a memory module controller ~~coupled to the plurality of memory devices~~ to enable a plurality of memory devices to be coupled to the system memory bus, the plurality of memory devices each having different signal quality requirements from each other, the plurality of memory module controller to receive a memory request signal from a system memory controller over a system memory bus, in response to the memory request, the memory module controller~~, which serves as an direct interface between the plurality of the memory devices and the system memory bus,~~ to generate a separate signal addressed to and served by at least one of the plurality of memory devices in a manner~~, such that the plurality of memory devices and the system memory bus operate in different operating environments~~, wherein the memory module controller separates the plurality of memory devices from the system memory controller and the system memory bus.

19. (Previously Presented) The memory module of claim 18, wherein the memory module controller further comprises a clock generator to generate a clock signal to drive

the separate signals controlling the plurality of memory devices, wherein the clock signal is different than a clock signal of the memory bus.

20. (Previously Presented) The memory module of claim 19, wherein the memory module controller further comprises a request handling logic to examine the memory request to determine whether the memory request is addressed to at least one of the memory devices and to ignore the memory request if the memory request is not addressed to any of the memory devices.

21. (Currently Amended) The memory of claim 20, wherein the memory module controller further comprises a power management unit to control [[a]] power supplied to the memory devices.

22. (Previously Presented) The memory module of claim 21, wherein the plurality of memory devices and the memory bus operate at different power voltages.

23. (Previously Presented) The memory module of claim 21, wherein the power management unit reduces at least a portion of the power to the memory devices, if the memory request is not addressed to any of the memory devices.

24. (Previously Presented) The memory module of claim 21, wherein the memory module controller further comprises a control logic coupled to the request handling logic, the clock generator, and the power management unit, the control logic configured to decouple the memory devices from the memory bus if the memory request is not addressed to any of the memory devices.

25. (Previously Presented) The memory module of claim 24, wherein in response to a signal from the request handling logic indicating that the memory request is not addressed to any of the memory devices, the control logic instructs the clock generator to alter a frequency of the clock signal to the memory devices.

26. (Previously Presented) The memory module of claim 25, wherein the control logic further instructs the power management unit to disable the clock generator if the memory request is not addressed to any of the memory devices, which in turn reduces the power dissipation of the memory devices.

27. (Previously Presented) The memory module of claim 18, further comprising a bus interconnecting the plurality of memory devices and the memory module controller, the bus having separate address, data, and control signal lines than the system memory bus.

28. (Previously Presented) The memory module of claim 18, wherein the memory module is a dual inline memory module (DIMM).

29. (Previously Presented) The memory module of claim 18, wherein the memory module is a single inline memory module (SIMM).

30. (Previously Presented) The memory module of claim 18, wherein the plurality of memory devices comprise one of volatile memory devices and non-volatile memory devices.